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EXAMINER

ZARNEKE, DAVID A

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/475,643
Filing Date: December 30, 1999
Appellant(s): JASSOWSKI, MICHAEL A.

Aslam Jaffery
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/28/06 appealing from the Office action
mailed 8/17/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. Note that Hiraga and Pendse reject both independent claims 1 and 44. In arguments section B with respect to Hiraga, only claim 1 is argued, but the same arguments would apply to claim 44. Further, in arguments section C with respect to Pendse, only claim 44 is argued, but the same arguments would apply to claim 1. This appears to be an over cite since sections H and K deal with dependent claims of the unmentioned independent claim.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Pendse et al., US Patent 5,818,114

Hiraga, US Patent 6,091,089

Hayashi et al., US Patent 5,581,109

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because the examiner has withdrawn them. The rejection of the claims over Hayashi et al., US Patent 5,581,109, has hereby been removed in view of the arguments presented. All other rejections remain as detailed below.

Claim Rejections - 35 USC § 102(b)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by

Pendse et al., US Patent 5,818,114.

Pendse (figure 3) teaches a semiconductor device, comprising:

a die having a first edge and a core;

a plurality of bond pads [316] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figure 3);

a first plurality of driver cells [314] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [312] located between the plurality of bond pads and the core.

Claim 44 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Pendse et al., US Patent 5,818,114.

Pendse (figure 3) teaches a semiconductor device, comprising:

a lead frame [abstract];

a die coupled to the lead frame, the die having

a first edge;

and a core;

a plurality of bond pads [316] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figure 3);

a first plurality of driver cells [314] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [312] located between the plurality of bond pads and the core.

Claim Rejections - 35 USC § 102(e)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5, and 6 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hiraga, US Patent 6,091,089.

Hiraga (figures 1A-1B & 3) teaches a semiconductor device, comprising:

a die [1] having a first edge and a core [2];

a plurality of bond pads [5 & 6] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figures 1B & 3);

a first plurality of driver cells [10] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [4] located between the plurality of bond pads and the core.

With respect to claim 3, Hiraga teaches a plurality of pre-drive cells located between the second plurality of driver cells and the core (5, 20-40).

In re claim 5, Hiraga teaches a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads (4, 4-12).

Regarding claim 6, Hiraga teaches a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects (5, 20-40).

Claims 44, 45, 47 and 48 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hiraga, US Patent 6,091,089.

Hiraga teaches a system comprising:

- a lead frame (2, 45+);

- a die [1] coupled to the lead frame, the die having

- a first edge;

- a core;

- a plurality of bond pads [5 & 6] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figures 1B & 3);

- a first plurality of driver cells [10] located between the first edge and the plurality of bond pads; and

- a second plurality of driver cells [4] located between the plurality of bond pads and the core.

With respect to claim 45, Hiraga teaches a plurality of pre-drive cells located between the second plurality of driver cells and the core (5, 20-40).

Art Unit: 2891

As to claim 47, Hiraga teaches each of the driver cells provides at least one of a drive strength, reception of incoming signals, and ESD protection of the core [column 4, lines 12+].

Regarding claim 48, Hiraga teaches each of the pre-drive cells provides communication between the core and one or more driver cells (4, 12+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3, 5-8 and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pendse et al., US Patent 5,818,114, as applied to claim 1 above.

With respect to claim 3, though Pendse fails to teach a plurality of pre-drive cells located between the second plurality of driver cells and the core, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of pre-

Art Unit: 2891

drive cells because pre-drive cells are conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

In re claim 5, Pendse teaches a plurality of metal connections [318a & 318b], each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads (figure 3).

Regarding claim 6, though Pendse fails to teach a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of conductive interconnects to couple the pre-driver cells to the driver cells because this is conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Regarding claim 7, though Pendse fails to teach each of the plurality of conductive interconnects substantially more narrow in width than each of the plurality of metal connections, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the relative widths of the conductive interconnects and the metal connects (MPEP 2144.05).

With respect to claim 8, though Pendse fails to teach the first and second pluralities of driver cells each have a width of approximately 80 microns, it would have

Art Unit: 2891

been obvious to one of ordinary skill in the art at the time of the invention to optimize the width of the first and second pluralities of driver cells (MPEP 2144.05).

In re claim 23, though Pendse fails to teach each of the conductive interconnects coupling a pre-driver cell to one of the first and second driver cells has a width ranging from approximately 1 -2 microns, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the width of the conductive interconnects (MPEP 2144.05).

Regarding claim 24, though Pendse fails to teach wherein at least one pre-driver cell is coupled to one of the first and second driver cells via multiple conductive interconnects, the mere duplication of parts has no patentable significance unless a new and unexpected result is produced (In re Harza, 124 USPQ 378 (CCPA 1960)).

With respect to claim 25, though Pendse fails to teach wherein at least one conductive interconnect is disposed on a layer other than a layer where the bond pads are disposed, the disposing of the conductive interconnect on a different layer is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

As to claim 26, though Pendse fails to teach wherein at least one conductive interconnect is disposed on different layer underneath at least one bond pad, it is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

In re claim 27, though Pendse fails to teach wherein at least one conductive interconnect is disposed on different layer underneath at least one driver cell, it is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

Claims 7, 8, and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraga, US Patent 6,091,089, as applied to claim 1 above.

Regarding claim 7, though Hiraga fails to teach each of the plurality of conductive interconnects substantially more narrow in width than each of the plurality of metal connections, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the relative widths of the conductive interconnects and the metal connects (MPEP 2144.05).

With respect to claim 8, though Hiraga fails to teach the first and second pluralities of driver cells each have a width of approximately 80 microns, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the width of the first and second pluralities of driver cells (MPEP 2144.05).

In re claim 23, though Hiraga fails to teach each of the conductive interconnects coupling a pre-driver cell to one of the first and second driver cells has a width ranging from approximately 1 -2 microns, it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize the width of the conductive interconnects (MPEP 2144.05).

Regarding claim 24, though Hiraga fails to teach wherein at least one pre-driver cell is coupled to one of the first and second driver cells via multiple conductive interconnects, the mere duplication of parts has no patentable significance unless a new and unexpected result is produced (*In re Harza*, 124 USPQ 378 (CCPA 1960))..

With respect to claim 25, though Hiraga fails to teach wherein at least one conductive interconnect is disposed on a layer other than a layer where the bond pads are disposed, the disposing of the conductive interconnect on a different layer is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

As to claim 26, though Hiraga fails to teach wherein at least one conductive interconnect is disposed on different layer underneath at least one bond pad, it is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

In re claim 27, though Hiraga fails to teach wherein at least one conductive interconnect is disposed on different layer underneath at least one driver cell, it is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

Claims 35-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pendse et al., US Patent 5,818,114, in view of Hayashi et al., US Patent 5,581,109.

Art Unit: 2891

Pendse (figure 3) teaches a semiconductor device, comprising:

a die having

a first edge, and

a core;

a plurality of bond pads [316] configured in an array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figure 3);

a first plurality of driver cells [314] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [312] located between the plurality of bond pads and the core.

While Pendse fails to teach a plurality of conductive interconnects to couple each of the plurality of pre-driver cells to one of the first and second pluralities of driver cells, wherein at least one conductive interconnects is disposed on a layer other than a layer where the plurality of bond pads are disposed, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of pre-drive cells because pre-drive cells are conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07). especially in light of Hayashi's teaching that the chip can be in a multi-layer form with interconnections between each layer (6, 30+).

Regarding the limitation that conductive interconnects that couple the pre-driver cells to the driver cells are disposed on a layer other than the layer that the bond pads

Art Unit: 2891

are disposed is merely an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)). The concept of placing interconnects underneath bond pads is more than well known in the art. This saves space on the chip surface and allows for more compact chips.

Regarding claim 36, Pendse teaches the plurality of bond pads are configured in a staggered array (figure 3).

With respect to claim 37, though Pendse fails to teach a plurality of pre-drive cells located between the second plurality of driver cells and the core, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of pre-drive cells because pre-drive cells are conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

As to claim 38, Pendse teaches the plurality of bond pads configured in the staggered array include an inner ring and an outer ring of bond pads (figure 3).

In re claim 39, Pendse teaches a plurality of metal connections [318a & b], each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

Regarding claim 40, though Pendse fails to teach each of the plurality of metal connections to couple one of the first and second driver cells to one of the bond pads has a width that is approximately up to 80 microns, it would have been obvious to one

ordinary skill in the art at the time of the invention to optimize the metal connections width (MPEP 2144.05).

With respect to claim 41, Pendse teaches each of the first driver cells is coupled to one of the outer ring of bond pads via one of the metal connections (figure 3).

As to claim 42, Pendse teaches each of the second driver cells is coupled to one of the inner ring of bond pads via one of the metal connections.

In re claim 43, though Pendse fails to teach at least one metal connection coupling a bond pad and a driver cell has a width equivalent to a width of one of the respective bond pad and the driver cell, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the relative metal connections width (MPEP 2144.05).

Claims 35-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraga, US Patent 6,091,089, in view of Hayashi et al., US Patent 5,581,109.

Hiraga (figures 1A-1B & 3) teaches a semiconductor device, comprising:

a die [1] having

a first edge,

and a core [2];

a plurality of bond pads [5 & 6] configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads (figures 1B & 3);

a first plurality of driver cells [10] located between the first edge and the plurality of bond pads; and

a second plurality of driver cells [4] located between the plurality of bond pads and the core.

Hiraga, which teaches a plurality of conductive interconnects to couple each of the plurality of pre-driver cells to one of the first and second pluralities of driver cells (5, 20-40), fails to teach at least one conductive interconnects is disposed on a layer other than a layer where the plurality of bond pads are disposed.

Regarding the limitation that conductive interconnects that couple the pre-driver cells to the driver cells are disposed on a layer other than the layer that the bond pads are disposed is merely an obvious matter of design choice, especially in light of Hayashi's teaching that the chip can be in a multi-layer form with interconnections between each layer (6, 30+). Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)). The concept of placing interconnects underneath bond pads is more than well known in the art. This saves space on the chip surface and allows for more compact chips.

Regarding claim 36, Hiraga teaches the plurality of bond pads are configured in a staggered array (figures 1B & 3).

With respect to claim 37, Hiraga teaches a plurality of pre-drive cells located between the second plurality of driver cells and the core (5, 20-40).

As to claim 38, Hiraga teaches the plurality of bond pads configured in the staggered array include an inner ring and an outer ring of bond pads (figures 1B & 3).

Art Unit: 2891

In re claim 39, Hiraga teaches a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads (4, 4-12).

Regarding claim 40, while Hiraga fails to teach each of the plurality of metal connections to couple one of the first and second driver cells to one of the bond pads has a width that is approximately up to 80 microns, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the metal connections width (MPEP 2144.05).

With respect to claim 41, Hiraga teaches each of the first driver cells is coupled to one of the outer ring of bond pads via one of the metal connections (4, 4-12).

As to claim 42, Hiraga teaches each of the second driver cells is coupled to one of the inner ring of bond pads via one of the metal connections (4, 4-12).

In re claim 43, though Hiraga fails to teach at least one metal connection coupling a bond pad and a driver cell has a width equivalent to a width of one of the respective bond pad and the driver cell, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the relative metal connections width (MPEP 2144.05).

Claims 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pendse et al., US Patent 5,818,114, as applied to claim 44 above.

With respect to claim 45, though Pendse fails to teach a plurality of pre-drive cells located between the second plurality of driver cells and the core, it would have been obvious to one of ordinary skill in the art at the time of the invention to a plurality of

Art Unit: 2891

pre-drive cells because pre-drive cells are conventionally known in the art. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

As to claim 46, Pendse teaches at least one of the first and second driver cells is an ESD (electrostatic discharge) cell (Figure 3, 314; [column 3, lines 50+]).

In re claim 47, Pendse teaches each of the driver cells provides at least one of a drive strength, reception of incoming signals, and ESD protection of the core [column 3, lines 50+].

Regarding claim 48, it would have been obvious to one of ordinary skill in the art at the time of the invention to use each of the pre-drive cells to provide communication between the core and one or more driver cells because this is inherently what pre-driver cells do, they provide communication between driver cells and the core.

Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraga, US Patent 6,091,089, as applied to claim 44 above, and further in view of Pendse et al., US Patent 5,818,114.

Hiraga fails to teach at least one of the first and second driver cells is an ESD (electrostatic discharge) cell.

Pendse teaches at least one of the first and second driver cells is an ESD (electrostatic discharge) cell (3, 50+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the ESD driver cell of Pendse in the invention of Hiraga because ESD protection is important in chip and package structures to protect the chip.

(10) Response to Argument

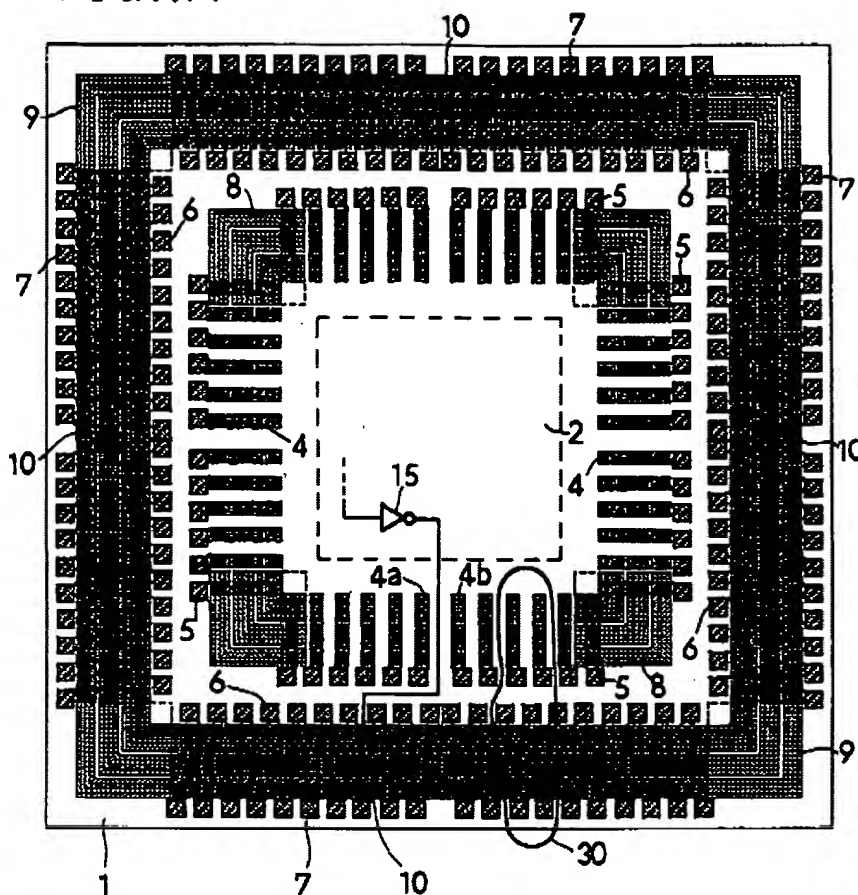
Applicant's arguments, with respect to Hayashi have been fully considered and are persuasive. The rejection of the claims has been withdrawn.

Applicant's arguments filed 3/38/06 with respect to Hiraga and Pendse have been fully considered but they are not persuasive.

The argument presented with respect to Hiraga is that it fails to teach the bond pads are a staggered array including an inner ring and an outer ring of bond pads.

Please note that Figures 1A, 1B and 3 of Hiraga clearly show that the bond pads 5 and 6 are staggered. With respect to the inner and outer ring, Figure 1A of Hiraga clearly shows the bond pads 5 and 6 form an inner and outer ring around the periphery of the die (1).

FIG. 1A



The argument presented with respect to Pendse is that it fails to teach the bond pads are a staggered array including an inner ring and an outer ring of bond pads.

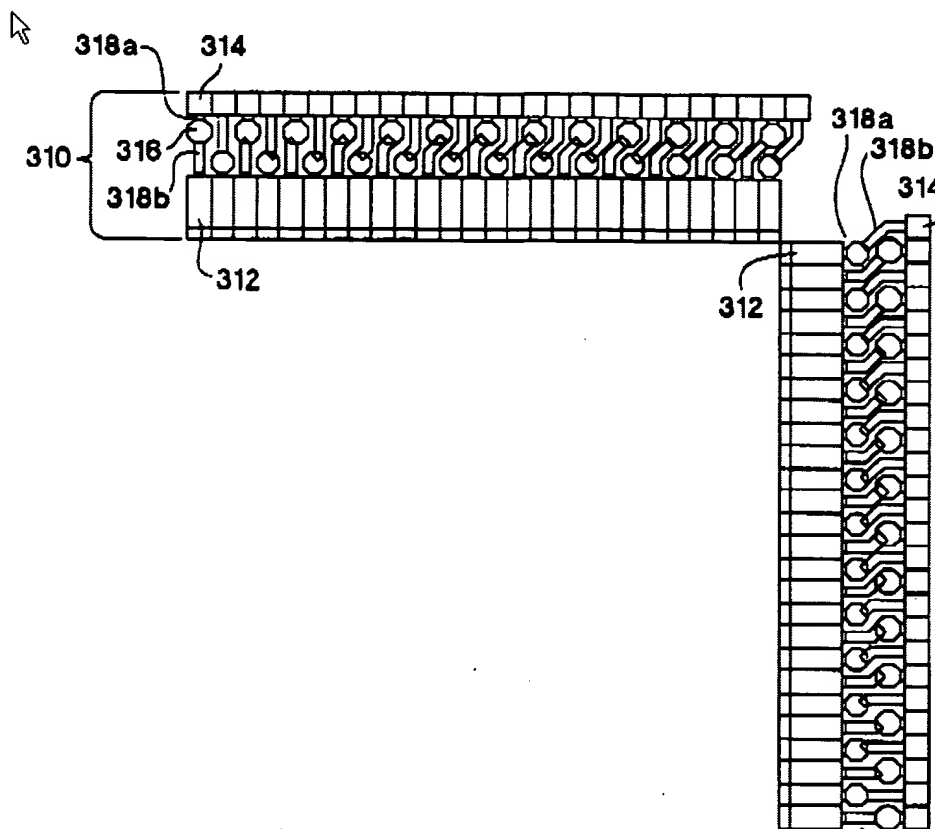
Please note that the specification (page 3, lines 57-59) and Figure 3 of Pendse clearly recite that the "bond pads 316 are radially staggered." With respect to the inner and outer ring, Pendse (page 3, lines 57-59) clearly states "the pad ring configuration of Fig. 3", which implicitly implies that Figure 3 is merely a partial showing of the die, wherein a Figure of the full die would have the bond pads 316 around the entire periphery. The inner and outer ring is clearly identified at the left side of Figure 3, where

Application/Control Number: 09/475,643

Page 20

Art Unit: 2891

the bond pads 316 nearest to the ESD structure 314 would be the outer ring and the bond pad 316 nearest the I/O circuitry 312 would be the inner ring.

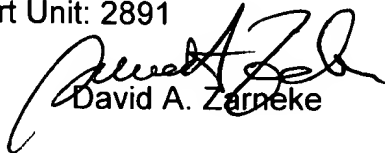
**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

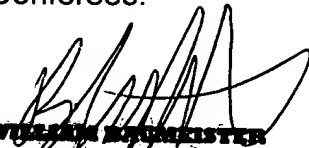
Respectfully submitted,

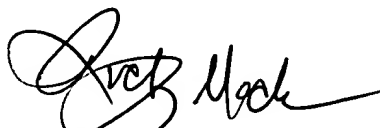
Art Unit: 2891


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